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Status and perspectives of crystalline silicon photovoltaics in research and industry

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Abstract | Crystalline silicon (c-Si) photovoltaics has long been considered energy intensive and costly. Over the past decades, spectacular improvements along the manufacturing chain have made c-Si a low-cost source of electricity that can no longer be ignored. Over 125 GW of c-Si modules have been installed in 2020, 95% of the overall photovoltaic (PV) market, and over 700 GW has been cumulatively installed. There are some strong indications that c-Si photovoltaics could become the most important world electricity source by 2040–2050. In this Review, we survey the key changes related to materials and industrial processing of silicon PV components. At the wafer level, a strong reduction in polysilicon cost and the general implementation of diamond wire sawing has reduced the cost of monocrystalline wafers. In parallel, the concentration of impurities and electronic defects in the various types of wafers has been reduced, allowing for high efficiency in industrial devices. Improved cleanliness in production lines, increased tool automation and improved production technology and cell architectures all helped to increase the efficiency of mainstream modules. Efficiency gains at the cell level were accompanied by an increase in wafer size and by the introduction of advanced assembly techniques. These improvements have allowed a reduction of cell-to-module efficiency losses and will accelerate the yearly efficiency gain of mainstream modules. To conclude, we discuss what it will take for other PV technologies to compete with silicon on the mass market.

Photovoltaics is a major actor of the ongoing energy transition towards a low-carbon-emission society. The photovoltaic (PV) effect relies on the use of a semiconducting material that absorbs light and converts it to free electrical charge carriers. Although several materials can be — and have been — used to make solar cells, the vast majority of PV modules produced in the past and still produced today are based on silicon — the second most abundant element after oxygen in the Earth's crust — in a crystalline form. In addition to a fast increase in volume manufacturing, one explanation for the success of crystalline silicon (c-Si) technologies in recent decades can be found in the easy way the manufacturing chain for c-Si from quartz to module can be split into separate steps (FIG. 1a). The perceived disadvantage of the numerous processing steps in c-Si PV technology compared with the easier processing of thin films has, over the years, turned into an advantage: each step can be, and has been, optimized quasi-independently with high volumes and high yields (typically >98% from wafer to cell), leading to significant cost reductions at all steps (FIG. 1b), as new manufacturers often focus on only one or two steps in the value chain — wafer, cell or module manufacturing, or system installation — instead of trying to consolidate the profit margins by vertical integration.

The history of Si photovoltaics is summarized in BOX 1. Over the past decade, an absolute average efficiency improvement of 0.3–0.4% per year has taken place, for both monocrystalline and multi-crystalline Si (FIG. 1c). The efficiencies of modules sold in 2021 typically range from 17.4% (low-grade multi-crystalline cells) to 22.7% (high-performance back-contacted cells)[1], with an estimated average of 20% for the most produced technology (passivated emitter and rear cell (PERC) monocrystalline). Note that, because of fast-evolving module designs, but also because existing lines are still being depreciated, the average efficiencies are lower than the state-of-the-art efficiencies. The newest mainstream, large modules will have efficiency values above 21%, but older-generation modules are still being produced with an average efficiency of 19%. The highest-efficiency modules (>22%) can require significantly more complex manufacturing,

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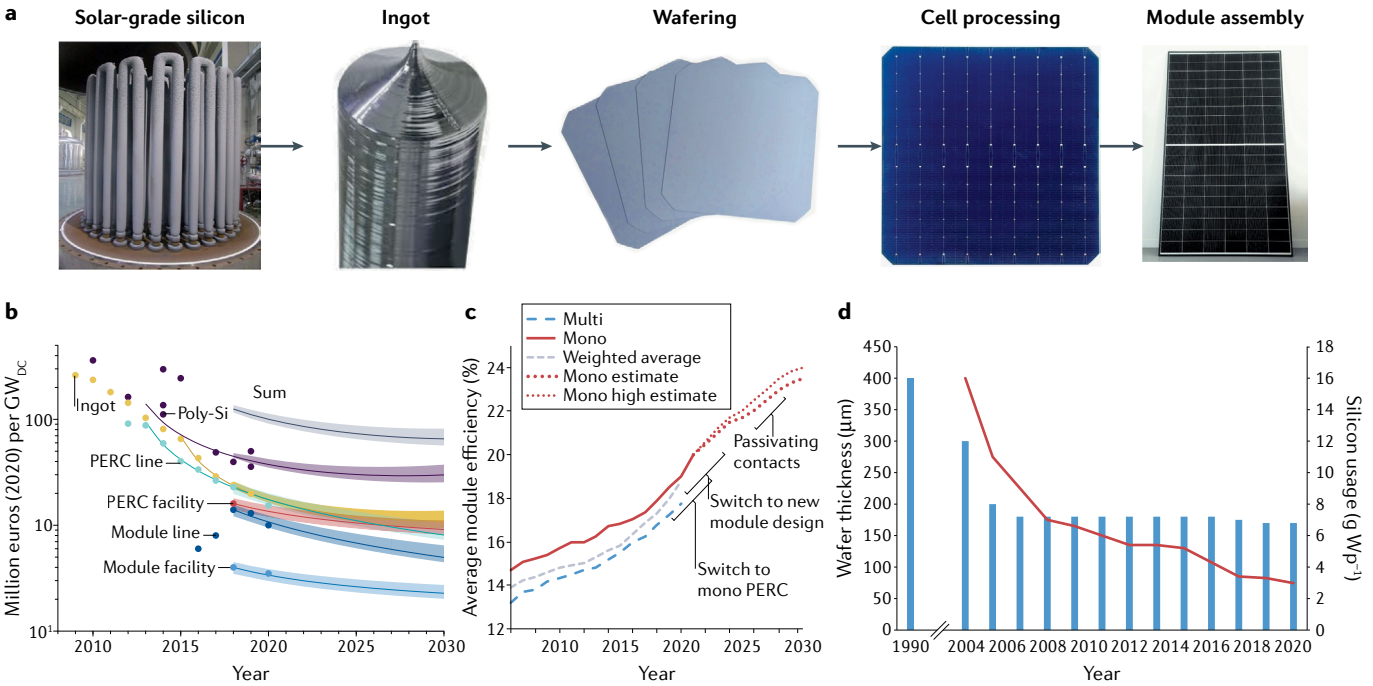

Fig. 1 | **From raw silicon to solar modules. a** | The main steps in making photovoltaic modules: purified polysilicon (poly-Si) preparation, crystalline ingot casting or pulling, wafering, solar cell processing and module assembly. **b** | Learning curve in capital expenditure along the value chain, from poly-Si purification to modules assembly. Symbols indicate historical data, lines indicate predicted future trends for passivated emitter and rear cell (PERC) cells. **c** | Average efficiency evolution of monocrystalline and multi-crystalline silicon mainstream modules, considering all modules sold on the market. An estimate for future improvements in the efficiency of monocrystalline cells is provided. **d** | Decrease in wafer thickness and silicon consumption over time. Panel **a** (Siemens reactor) adapted with permission from REF.[229], Elsevier. Panel **a** (ingot) courtesy of LONGi. Panel **b** adapted with permission from REF.[230], P. P. Altermatt. Panels **c** and **d** adapted with permission from REF.[231], Fraunhofer ISE.

which increases their cost and price by a factor of 2 to 3. They are, thus, mostly relevant for niche applications (such as rooftop or remote systems), for which the efficiency and power density are more important than the levelized cost of the produced electricity.

The question of whether efficiency improvements and cost decreases will keep their pace is crucial for the prospects of photovoltaics as a global energy source. In this Review, we explain why and how this trend is likely to continue, based on a detailed analysis of the evolution of the material technology and present trends in research and development.

We start by reviewing the key elements that have enabled silicon photovoltaics to become a low-cost source of electricity and a major actor in the energy sector. Material usage reduction and wafer quality improvement, jointly with a spectacular price decrease, were simultaneously achieved in the past decades. We then discuss how the industry's favourite cell technology has evolved in the past few years from the historical structure described in the 1970s towards a better-performing PERC structure. We further discuss how, following the demand for high-performing and low-cost PV systems, even more efficient cells relying on passivating contacts are currently being rapidly developed with strong industrial involvement. We then survey the recent evolution of modules that enabled a reduction of cell-to-module efficiency losses, particularly in the past couple of years. Over the past decade, mainstream module efficiency increased by 0.3–0.4% absolute per year on average, now reaching efficiencies of 19–22%. The improvements discussed here notably enable today's modules to generate the energy needed to fabricate them in much less than one year. Based on present-day knowledge, we describe the technological innovations that will enable the cost of PV electricity to routinely reach US$0.013–0.03 kWh^{-1} within the next decade all around the globe. Finally, we briefly discuss how alternative PV technologies could compete with silicon on the mass market.

From polysilicon feedstock to wafers

For high-efficiency PV cells and modules, silicon crystals with low impurity concentration and few crystallographic defects are required. To give an idea, 0.02 ppb

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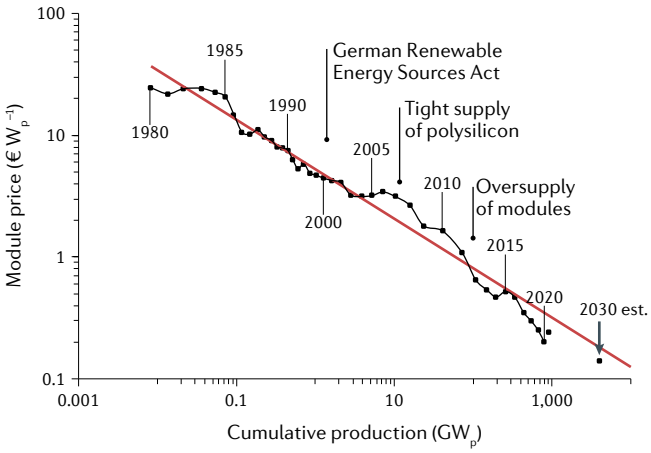
of interstitial iron in silicon, corresponding to a concentration of around 10^{12} cm^{-3}, can bring a c-Si solar cell efficiency from 20% down to ~12%, as excited electrons lose their energy to iron-related recombination centres. The required purification of the silicon feedstock and cleanliness of the following processes are comparable with specifications in microelectronics.

Silicon processing starts with metallurgical-grade silicon (with ~1% impurities), which is reacted with HCl to create trichlorosilane ($SiHCl_3$ or TCS), a liquid with a boiling point of 32 °C. A series of distillation cycles (typically 3–5) is used to obtain TCS with a purity of 9N to 12N, that is, with less than one impurity per billion atoms (one per trillion in the 12N case). Subsequently, TCS is fed together with H_2 into a cooled-wall reactor, in which high-purity silicon filaments (a few millimetres in width) are heated to 1,150 °C. TCS dissociates thermally at the surface of the hot silicon filaments, and silicon deposition thickens the filaments to rods of 10–20 cm in diameter. This process, usually called the Siemens process, is a costly and energy-intensive part of the silicon PV chain, but improvements in internal jar reflective coatings and increases in reactor size reduced its cost and energy requirements. Up to 10 tons of high-purity silicon can now be produced in ~100 h in the largest reactors, with an energy consumption of 35–45 kWh kg^{-1} (REF.[2]). The silicon rods are then crushed into chunks and used for the growth of silicon ingots. Depending on the number of distillation cycles, which impacts the material quality, the price of solar-grade silicon was typically in the range US$6–7 kg^{-1} for low-quality silicon and up to US$10–12 kg^{-1} for high-quality silicon in 2020. Further cost reduction is possible[2], for instance, by using larger tubular silicon filaments, which reduce

Box 1 | **A historical perspective**

The Bell Laboratories in the USA demonstrated the first solar cell of practical interest, with 6% efficiency, in 1954 (REF.[237]). In the following years, the main market driver for silicon cells was space applications, whereas the terrestrial market was limited mostly to off-grid applications. The small manufacturing volumes translated into high prices, preventing any massive deployment of photovoltaics. The first terrestrial photovoltaic (PV) power plant, of 1 MW in capacity, was built in 1982.



In the years from 1980 to early 1990, the most important technological bricks for the realization of high-performance and/or industrial silicon solar cells were developed, building on microelectronics and power semiconductor technologies. Monocrystalline solar cells reached efficiencies of 20% in the laboratory in 1985 (REF.[238]) and of 26.2% under 100× concentration in 1988 (REF.[239]). In this period, the efficiency of industrial solar cells slowly grew from 12% to 14.5%. The challenge was still to find a way to go from, for example, US$4–5 W^{-1} in 1994 (REF.[240]) down by a factor at least 10 to make photovoltaics a competitive electricity source, a goal that required technology improvements, larger production volume and a dedicated supply chain. Globally, many countries provided significant contributions to the PV industry in the past 50 years: first, the USA with its large PV market for satellites and the first large-scale PV plants, then Australia with its large, remote PV-powered telecommunication market and Japan with the first significant residential PV market. A large acceleration took place at the beginning of the twenty-first century, with innovative and significant feed-in tariffs in Germany and many European countries[241], which triggered a vast effort of EU equipment makers, enabling enhanced manufacturing capability for the industry. Finally, China played a major role in manufacturing, through large financial support from international investors, particularly from the USA, which supported low-cost mass industrialization.

The incentive schemes triggered, from 2000 to 2010, a strong market growth of over 30% per year, and had profound effects. For the first time in 2004, the PV industry used more silicon (in weight) than the entire semiconductor industry, leading to a shortage of refined polysilicon from 2004 to 2009. The price of solar-grade polysilicon feedstock reached US$400 kg^{-1}, up from US$30–50 kg^{-1} before the shortage. This triggered investment in large polysilicon production plants, enabling prices as low as US$6–12 kg^{-1} in 2021. In parallel, the production capacity increased for solar cells and solar modules, mainly in Asia and, in particular, in China, leading to global overinvestment and oversupply. The selling price of modules dropped fast in 2010–2015, forcing many companies out of business. The mass industrialization proceeded with a volume growth of around 25% per year over the past decade, exceeding 130 GW in 2020. This corresponds to an area of 630 km^2 of crystalline silicon modules, representing over 95% of the PV market[10]. From 1980 to 2020, PV module prices decreased by 24% for each doubling of the cumulated produced capacity (see the figure). Assuming constant margins, this suggests a learning rate of 24% over the past four decades also in terms of cost. A learning rate of 40% can be observed for the past decade, explained by the recovery from the early 2000s shortage followed by the concentration of a manufacturing cluster in China, and standardization of tools, processes and designs throughout the entire supply chain. Today's typical wholesale price for mainstream crystalline silicon modules is in the range US$0.17–0.25 W^{-1} (REF.[10]), depending on the type and efficiency, which converts to a staggering low US$35–50 m^{-2}.

Data until 2021 adapted with permission from REF.[10], Fraunhofer ISE.

Box 2 | **The different kinds of silicon**

Silicon wafers used for photovoltaics can be distinguished by the way they have been crystallized. Over the past two decades, multi-crystalline silicon (mc-Si) wafers made by directional solidification (DS) have represented, on average, about 60% of the market. In DS, the molten silicon is slowly crystallized from bottom to top in a square-shaped crucible made of fused silica coated with silicon nitride (SiN_x) (see the figure, left panel). Every solidification requires a new crucible. The bottom of the crucible contains seeds to influence the crystal growth[38,242,243]. This 'incubation layer', made of small pieces of silicon, silicon dioxide, silicon nitride, silicon carbide or other high-temperature materials, is used as a seed to obtain relatively small grains of typically a few millimetres that relax crystallographic dislocations more easily than large grains. This type of Si is referred to as high-performance multi-crystalline ('HP-multi') material. Alternatively, the use of monocrystalline seeds results in large parts of the ingot having a monocrystalline structure ('quasi-mono' or 'cast-mono' material) (see the figure, middle panel)[244]. The size of the crucibles is continuously increasing: ingots of up to 1,650 kg can be solidified.

Driven by the development of high-efficiency passivated emitter and rear cell solar cells, which require substrates of better quality, and recent improvement in the Czochralski (Cz) process, which enables multiple recharge and multiple-ingot pulling, the year 2018 has seen a significant change in the silicon wafer market. The major share of the current market is now based on monocrystalline ingots grown via the Cz method (see the figure, right panel). Here, a seed crystal is dipped into molten silicon contained in a rotating quartz crucible and slowly pulled upwards, resulting in a ~2-m-long, cylindrically shaped single crystal of typically 200–300 mm in diameter. The crucible can be recharged while still hot and three to five ingots can be pulled without cooling and breaking the controlled atmosphere[245–247]. Eventually, detrimental metal impurities accumulate in the melt owing to their higher solubility in the liquid phase and the crucible with the residual melt must be changed. The fracture strength of the seed crystal, with its typical diameter of 3 mm, limits the maximum ingot weight and, thus, its length.

The DS process yields Si ingots at a lower cost than the Cz method thanks to a higher throughput and lower energy consumption. DS silicon is, however, so far, more defective than Cz silicon due to impurity diffusion from the crucible, but also precipitates, dislocations and grain boundaries that depend on the position in the ingot and on external parameters, such as the cooling rate. However, the quality of silicon can be significantly improved during cell fabrication. As an indication, the world record solar cell efficiencies for DS ingots are 22.8% for mc-Si and 24.4% for quasi-mono Si (REF.[74]). Conversely, the main impurities in Cz ingots are oxygen and carbon, which can reach concentrations up to $10^{18}\,cm^{-3}$ and $5\times10^{16}\,cm^{-3}$, respectively[248]; lower concentrations are possible by a careful design of the puller[7]. The float-zone crystal growth technique, often used to reach high performances in laboratories, is currently not used in the photovoltaics industry owing to cost considerations and material-quality improvements of Cz silicon.

Several wafering technologies that avoid the ingot sawing step are under development. In direct epitaxy[249], a monocrystalline silicon substrate is treated to form a porous silicon layer. Following a heat treatment, epitaxial silicon is deposited to the desired thickness using silane or chlorosilanes. Afterwards, the grown layer can be lifted off[250]. For ribbon silicon[251], a thin sheet of mc-Si is pulled from the melt and cut into wafers. The Direct Wafer technology[252] grows multi-crystalline wafers from the melt by selectively cooling the surface and lifting off the solidified sheet.

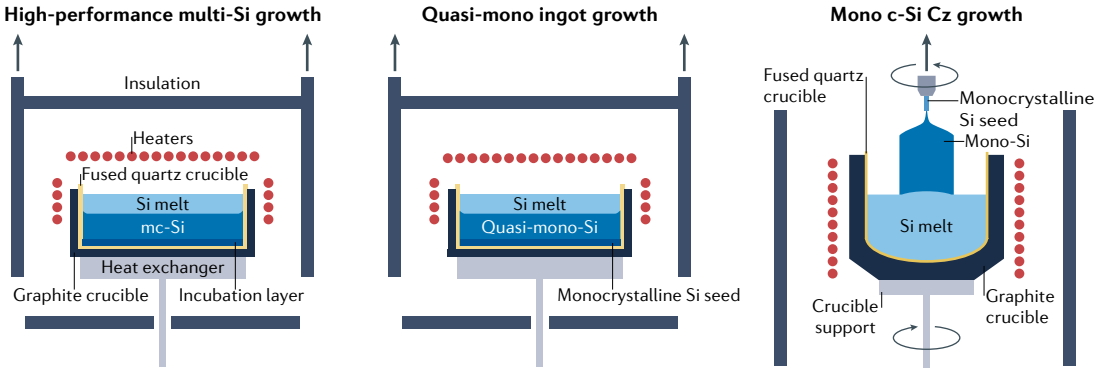


Figure courtesy of M. Lehman.

the deposition time thanks to their increased initial surface area[3]. Fluidized bed reactors constitute an alternative approach to deposit silicon and could halve the energy needs for this step[4], but they have a small market share[5]. With state-of-the-art processes and starting from sand, the total electricity consumption to produce 1 kg of purified polysilicon feedstock amounts to about 60 kWh (11 kWh kg^{-1} for making metallurgical-grade silicon, 49 kWh for purifying and producing polysilicon).

Two principal techniques are then used for the preparation of silicon ingots (BOX 2): directional solidification (DS) and the Czochralski (Cz) method[6,7], with the Cz method using roughly four times more electricity than the DS technique (32 versus 7 kWh kg^{-1} of crystallized silicon). Blocks and ingots are subsequently cut into (pseudo-)square bricks with typical edge lengths of 156–210 mm and then sawn into wafers using the multi-wire sawing technique. Here, a thin steel wire is wound multiple times around guiding cylinders to saw simultaneously up to several thousand wafers. The original process developed in the 1980s used a slurry of silicon carbide particles in glycol solution to chip through the silicon[8]. This process had significant kerf losses (the wire diameter plus twice the diameter of the silicon carbide particles), adding up to 120–200 µm. Between 2015 and 2019, diamond wires (steel wires bonded with

microparticles of diamond) became the new standard[9], reducing kerf losses to 50–70 µm and significantly contributing to the reduction of wafer price in recent years. Combined with reduced cell thickness and increased cell efficiency, the amount of raw silicon decreased spectacularly from 14 g W^{-1} in 2000 to 3.0 g W^{-1} today (FIG. 1d, all power values refer to peak power under standard test conditions). Summing up all electricity consumption for going from sand to wafer yields just under 100 kWh kg^{-1} (including 5 kWh m^{-2} for wafer sawing), that is, 0.3 kWh W^{-1}. This energy expenditure is compensated in the field in 2 to 4 months, depending on the irradiance. Altogether, the energy payback time for silicon PV systems amounts nowadays to less than 1 year in southern European countries (1.2 years in northern Europe) for a standard mounting for both DS and Cz growth technologies, with a slight advantage for silicon grown by DS due to the lower energy requirements[10,11], and is well below 1 year considering only the module part.

As a result, the cost of silicon wafers per m^2 of module area is now astonishingly low compared with just 10 years ago. With a typical wafer thickness of 170 µm, in 2020, the selling price of high-quality wafers on the spot market was in the range US$0.13–0.18 per wafer for multi-crystalline silicon and US$0.30–0.35 per wafer for monocrystalline silicon, which, with a typical size of 158.75 × 158.75 mm^2, corresponds to US$6–13 m^{-2}. This price sets a high benchmark for the alternative wafering techniques discussed in BOX 2. Noticeably, a strong demand for Si feedstock has led to a sharp price increase in 2021 by a factor of 2 to 3 (BOX 1). Together with a PV glass shortage, this has contributed to a price increase along the full chain of photovoltaics, which is anticipated to come down again in 2022 and 2023 with the addition of new capacity.

Carrier lifetime in silicon

The indirect bandgap of silicon yields only a moderate absorption and, thus, requires a wafer thickness of 100–200 µm to absorb most of the light with energy above the bandgap. For the photo-generated minority carriers to diffuse towards the selective contacts with a minimum of recombination losses, the (effective) minority charge carrier diffusion length L_{eff} should be several times larger than the thickness of the wafer; L_{eff} is defined in terms of the minority charge carrier diffusivity D and the effective excess charge carrier lifetime τ_{eff} as $L_{eff} = \sqrt{D \cdot \tau_{eff}}$. Long lifetimes require a low level of recombination losses.

The recombination losses come not only from the bulk properties (BOX 3) but also from dangling bonds at the surfaces. Through chemical surface passivation, these dangling bonds can be bonded with other atoms, for example, with oxygen when the surface is passivated with silicon dioxide. Hydrogen also passivates dangling bonds very effectively. However, hydrogen passivation can be unstable under heat or ultraviolet (UV) light. By contrast, field-effect surface passivation relies on layers with suitable polarity of fixed charges (positive charges for n-type surfaces, such as SiN_x, or negative charges for p-type surfaces, such as Al_2O_3), which accumulate majority carriers and deplete the surface of minority carriers through band bending, thus, reducing recombination by removing one type of carrier from the surface[12]. Surface passivation can, in principle, also be achieved by inversion, but this type of passivation is less efficient than accumulation, is more sensitive to charge variations and can be destroyed when the layer is locally opened for contacting due to parasitic shunting[13,14].

Increasing effective lifetime during processing. The density of defects within the wafer bulk can significantly change during solar cell processing. Depending on processing temperatures, precipitates can be dissolved or

Box 3 | Key losses in a silicon solar cell

A perfect solar cell would have no losses apart from the ones dictated by physics or thermodynamics. In a semiconductor, photons with energy lower than the bandgap are not absorbed. For absorbed photons, the part of their energy exceeding the bandgap is dissipated into heat in a process called thermalization. The theoretical efficiency limit of a solar cell is then governed by radiative recombination, which is the reciprocal process of absorption. For a semiconductor with a bandgap of 1.1 eV, this process yields a limiting efficiency of 32%[253,254]. For crystalline silicon, the limiting recombination process is not radiative recombination but Auger recombination, which is independent of how pure and perfect the substrate is. To assess the maximum theoretical efficiency, it is, therefore, mandatory to accurately determine the parameters of the Auger process. Several models have been proposed[255–257], placing the efficiency limit around 29.5%[256–258]. In addition to these fundamental loss mechanisms, other practical losses limit the efficiency of real solar cells. These include recombination at defects, optical losses and resistive losses.

Recombination losses in the bulk are assessed by measuring the bulk lifetime τ_{bulk} of excess charge carriers. The crystal surfaces at the front and rear contribute additional recombination losses that are generally expressed by the surface recombination velocities S_f and S_r. A thermal oxidation of the surface is an excellent way to reduce the carrier recombination at the interface. For many years, this process step had been considered too expensive to be used in industrial manufacturing of low-cost solar cells. It has, however, been recently introduced in large-volume manufacturing before silicon nitride (SiN_x:H) deposition. Traditionally, the low-cost method to reduce the carrier recombination at the interfaces was to introduce a high–low doping profile that reduces the minority-carrier density at the interface, for example, in the back-surface field. Field-induced accumulation or inversion layers have the same effect of reducing the effective surface recombination. Current high-efficiency silicon solar cells combine a thin silicon oxide layer with positive charges with a layer of SiN_x:H for n-type Si or with negative charges with a layer of Al_2O_3 for p-type Si.

All recombination pathways add up in parallel, leading to the definition of an effective carrier lifetime τ_{eff}, which, in the case of a uniform carrier concentration across a device with reasonably good surface passivation, can be written as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} = \sum_i \frac{1}{\tau_{bulk,i}} + \frac{S_f}{W} + \frac{S_r}{W}$$

where τ_{bulk} contains contributions of radiative recombination, Auger processes and trap-associated carrier lifetimes, whereas $\tau_{surface}$ is defined in terms of S_f and S_r and the device thickness W. A high value of τ_{eff} assures low recombination rates of the generated excess charge carriers and, thus, enables building up a high internal voltage.

Optical losses occur by shading of the metal contacts (~3–4%), surface reflection (~3%), parasitic absorption in dielectric layers and contacts (<1%), free-carrier absorption (<1%) or imperfect light management (<1%). A good light-trapping scheme, combining anti-reflection coating, surface texture, good internal surface reflectivity, highly reflective metals for infrared wavelengths and low doping to avoid free-carrier absorption, should be applied to significantly increase the path length of weakly absorbed, long-wavelength photons and to guarantee that they can be absorbed in the silicon crystal. In addition, sub-bandgap photons of wavelengths greater than 1,200 nm should ideally be reflected to avoid unnecessary heating of the solar cell.

Series resistance can be another significant source of power loss, in particular, in the emitter, the metal fingers and the interconnection. These losses are mitigated through continuous technology improvements, such as decreasing finger pitch (while decreasing finger width to maintain a low shadowing), multi-busbar or wire interconnection (9 to 20) and cutting cells in half or even in smaller sub-cells.

formed, depending on their solubility and diffusivity[15], and gettering processes can remove transition metals by attracting and collecting them into 'sinks' with higher solubility[16]. Internal gettering refers to segregation in extended defects or highly doped regions, whereas external gettering utilizes layers at the wafer surface, such as a doping glass[17] or a SiN_x:H layer[18].

Besides its role in surface passivation, hydrogen also has a positive impact on bulk recombination. It can be introduced by a H-rich SiN_x:H layer deposited by plasma-enhanced chemical vapour deposition (PECVD), followed by a short annealing (firing) to release the hydrogen into the bulk silicon. Hydrogenation is effective in improving areas of higher defect density, conveniently supporting the improvements achieved by gettering, although the local defect structure is very important[19]. Hydrogenation was also found to improve τ_{eff} more effectively in cleaner samples, especially when reducing the recombination activity of grain boundaries[20–22].

Bulk lifetime degradation phenomena. Reaching a high τ_{eff} at the end of the solar cell fabrication process is important, but it is not sufficient to ensure a long-lasting and efficient solar electricity production. For example, boron-doped p-type c-Si with high oxygen concentration, such as in a Cz material, is vulnerable to degradation under illumination[23]. This effect reduces τ_{eff} within several hours of carrier injection; it scales almost linearly with boron concentration and roughly quadratically with interstitial oxygen concentration[24,25]. This process was termed boron-oxygen (BO)-related light-induced degradation (LID), which is misleading because it also occurs under biasing of cells in the dark, as only the presence of excess charge carriers is needed, not the photons themselves. A fundamental lifetime limit imposed by BO-LID was established by studying bulk lifetime after full degradation[26]. In 2006, it was discovered that lifetime after BO-LID can be regenerated by a process involving excess charge carriers at 150–300 °C in the presence of hydrogen in the sample[27,28]. The kinetics of the degradation–regeneration cycle can be described by a three-state model (annealed, degraded and regenerated state)[29] and more generalized models[30]. The defects can be deactivated by exposure to a high light intensity at above 200 °C for less than 1 min (REFS[31,32]) or by biasing the cell at around 200 °C in the dark (for example, in a stacked configuration)[33,34]. The deactivation is stable long term, thus, BO-LID is no longer the dominant limitation of boron-doped Cz silicon solar cells. Additionally, gallium recently almost completely replaced boron for fabrication of p-type wafers, thus, avoiding BO-LID issues, even though gallium distribution in the ingots is less homogeneous than boron distribution[35].

Another degradation mechanism in bulk silicon, discovered in 2012 (REF.[36]), occurs on measurable timescales only above room temperature, mainly in p-type materials. Therefore, it was termed LeTID (light- and elevated-temperature-induced degradation). Similar to BO-LID, it is based on the presence of excess charge carriers, but does not have a clear dependency on doping or oxygen level[37], and a regeneration can be observed, too. The effect is more pronounced in multi-crystalline material[36] (FIG. 2a), where its strength can be influenced by gettering and the local defect structure[38,39], but it

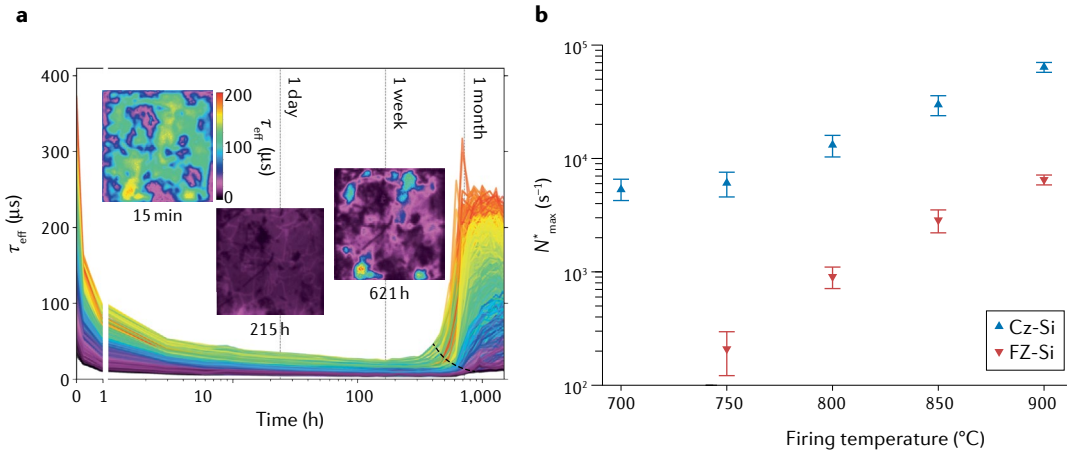


Fig. 2 | **Defect creation in silicon as a function of light and temperature. a** | Spatially resolved effective charge carrier lifetime (τ_{eff}) of a p-type 5 × 5-cm^2 multi-crystalline Si sample under 75 °C and 1 sun illumination measured using time-resolved photoluminescence imaging[38]. Each line represents the τ_{eff} of a 100 × 100-μm^2 sample area, with the colour code scaled to the value before illumination. All wafer areas show a severe light- and elevated-temperature-induced degradation effect, with areas of higher initial material quality regenerating earlier than poor-quality areas (dashed line). Inset: lifetime maps at different points in time. At maximum degradation (around 215 h), areas near grain boundaries show longer lifetimes than the neighbouring grains. The first hour is shown on a linear scale, the rest on a logarithmic scale. The SiN_x:H surface passivation layer was deposited by plasma-enhanced chemical vapour deposition and fired at 800 °C peak sample temperature. **b** | Maximum equivalent defect concentration N^*_{max} during a degradation experiment using boron-doped Czochralski (Cz) and float-zone (FZ) Si wafers coated with SiN_x:H (REF.[232]). Higher firing temperatures lead to increased N^*_{max}, possibly owing to increased concentrations of hydrogen in the silicon bulk. Note that, for Cz-Si, both phenomena, light- and elevated-temperature-induced degradation and boron-oxygen-related light-induced degradation, are present, resulting in a higher N^*_{max} compared with FZ-Si. Panel **a** adapted with permission from REF.[38], Wiley. Panel **b** adapted with permission from REF.[232], AIP.

is also observed in Cz (including gallium doped) and even higher-purity float-zone (FZ) material[40,41] (FIG. 2b). Recently, LeTID was also reported for sample structures based on n-type wafers, provided they contain highly doped p-type or n-type layers[42], whereas samples with moderate n-type doping seem to be unaffected[41]. The presence of hydrogen in the silicon bulk is presumed to be a prerequisite for the defects to form[43], and peak firing temperatures and ramping rates have a strong impact on the strength of LeTID[39,44] (FIG. 2b). Early models assumed that a diffusing species is involved in the process[44]. More recent findings resulted in a four-state model with a 'reservoir' state determining the availability of defect precursors for degradation[45]. Possible measures to avoid LeTID in p-type solar cells are the use of lower firing temperatures or thinner wafers[44], although neither appears to be compatible with current industry needs. Thermal treatments in the dark or under carrier injection might be more suitable for implementation in mass production. As regeneration timescales are longer than for BO-LID, LeTID remains a severe problem for p-type solar cell processing. Many manufacturers found mitigation strategies resulting in reduced degradation strengths[46], but all need extra steps and/or increase processing cost.

The vulnerability of p-type silicon to these degradation phenomena brought back the 60-year-old discussion about whether p-type or n-type silicon is better suited for solar cell production. Early silicon cells were made on n-type wafers, but when space applications became a large market, p-type silicon was favoured because of a better resistance to electron irradiation in orbit. Subsequently, p-type remained the substrate of choice, mostly because the rear metallization with aluminium conveniently forms a contact and a back-surface field (BSF) simultaneously. However, long lifetimes are easier to reach with n-type material and most cells with high efficiency (>23%) rely on long bulk lifetimes (>1 ms)[47]. In terms of processing, solar cells based on n-type silicon show a slightly higher complexity and higher manufacturing cost, as both phosphorus for the BSF and boron for the emitter (the region of the wafer showing opposite doping from the bulk)[48] have to be diffused, and because both front and rear metal layers require silver-based pastes. The boron-doped emitter might also cause problems, because its formation might generate oxygen-related defects. This issue can be avoided by a preprocessing step at high temperature, typically more than 1,000 °C, to dissolve oxygen precipitates (called tabula rasa)[49], but at the cost of adding process complexity, which prevents its use in industrial production.

Solar cell processing

Most silicon solar cells until 2020 were based on p-type boron-doped wafers, with the p–n junction usually obtained by phosphorus diffusion, and, until 2016, they were mostly using a full-area Al-BSF (FIG. 3a), as first described in 1972 (REFS[50–52]). Since then, constant cost decrease and efficiency increase followed from multiple small but important improvements. The main ones are screen-printing of metal contacts, effective surface textures, positively charged silicon nitride surface passivation and selective emitters.

A major challenge in c-Si technology consists in applying metallic electrodes to extract the charge carriers. Because of the high defect density at direct metal–semiconductor interfaces, the contacts are an important source of recombination. There are two main options to limit their impact, giving rise to the various device structures illustrated in FIG. 3.

The first option is to reduce the metal–Si contact area. The remaining metallized areas should have low contact resistivity, and the surface between the contacts should be passivated[53,54]. Using photolithography to define the coverage fraction and controlling the doping profile in the adjacent regions in the wafer, this concept resulted in the first silicon solar cell with a 25% designated area efficiency in 1999 (REF.[55]). Usually, called PERC following REF.[56], a simplified version of this design, shown in FIG. 3b, is at the heart of current mass production.

The second option is to separate the metal electrode from the Si wafer. In this case, a stack of a passivating film (to reduce the density of interface defects) and a doped film (to selectively conduct only one polarity of charges) are inserted between silicon and the metal. Balancing the passivation characteristics and the contact resistance is the most difficult aspect of these 'passivating contacts'. The most widely used stacks consist of intrinsic and doped amorphous silicon[57] (FIG. 3g,h) or of silicon oxide and polysilicon[58–60] (FIG. 3e,f). Passivating contacts have enabled the most recent record efficiencies beyond 25%[61].

Al-BSF cell processing. The typical industrial Al-BSF cell processing, predominant until 2017–2018, is presented in the left part of FIG. 4. Starting with boron-doped p-type wafers, a light-scattering texture is etched by wet chemistry. For monocrystalline wafers with (100) crystallographic orientation, random upright pyramids are obtained by anisotropic etching in caustic solutions, whereas for multi-crystalline material, isotropic etching in acidic solutions yields hemispherical pits. Next, the n-type emitter is formed using a $POCl_3$-based phosphorus diffusion at around 800–850 °C, generally in quartz tube furnaces with batches of about 1,200 wafers that are loaded back to back. The phosphorus atoms diffuse less than 0.5 µm into the Si bulk with a diffusion profile that is optimized as a trade-off between lateral conductivity and emitter recombination. The phosphorus–silicate–glass layer formed at the surface of the wafer during the diffusion and the parasitic P-diffused region at the rear are etched away using wet chemistry. During the same etching step, the rear surface is chemically planarized. Next, PECVD is used to deposit a SiN_x:H layer on the emitter, where it acts as an anti-reflective coating and as a positively charged surface passivation layer.

Subsequently, a multistep screen-printing process is used to form the metal contacts. First, a silver paste is screen-printed to form the soldering pads at the rear of the cell. After drying, the rear surface is printed with an aluminium paste that may contain additional boron. After drying and flipping the cell, the front surface is printed with a paste that contains silver and glass frit to

form the front metallization. The next processing step is the co-firing in a belt furnace at a peak wafer temperature of around 800 °C, where several things happen simultaneously. On the rear of the wafer, aluminium melts and dissolves silicon. During cool-down, silicon recrystallizes according to the Al/Si phase diagram[62], incorporating aluminium and boron (if added to the paste) with concentrations up to their solubilities in the solid. This forms a highly doped p-type BSF region. The remaining aluminium eventually solidifies to form the rear contact. On the front side, the glass frit etches through the SiN_x:H layer, enabling contact formation between the silver and the highly doped n-type emitter surface[63]. Another important phenomenon during co-firing is the release of hydrogen from the SiN_x:H layer. Hydrogen can passivate the numerous dangling bonds at the c-Si–SiN_x:H interface, as well as some crystal defects in the bulk of the silicon wafer.

Finally, current–voltage measurements are performed in the dark and under '1 sun' illumination; this last measurement enables the extraction of the conversion efficiency and of the main parameters of the cell: the open-circuit voltage (V_{oc}), the short-circuit current (I_{sc}) and the fill factor (FF), which is defined as the maximum power output divided by the product of V_{oc} and I_{sc}. The reverse current–voltage characteristics and the reverse breakdown voltage are also tested. The cells are then sorted in a matrix of bins as a function of their efficiency and short-circuit current with company-dependent strategies. In most high-quality industrial production lines, the electroluminescence image of every cell is recorded and checked for micro-cracks or other defects, and the cells are additionally sorted by colour variation.

Evolution towards PERC and other designs. A first evolution introduced into industrial Al-BSF cell manufacturing around 2005–2010 was a selective emitter design[64]. This design includes a heavily doped emitter under the metal contacts and a lightly doped emitter between the metal contacts. Selective emitters simultaneously enable a good electrical contact and a low average emitter recombination. They are manufactured either by using a laser doping process that enhances doping under the contacts or by an etch-back process in the area between the contacts. Significant progress was made over the past decade on silver pastes and new formulations enable good contacting of very lightly doped emitters, which, combined with narrower line printing (currently less than 40 µm), reduces recombination in the emitter region[65] and

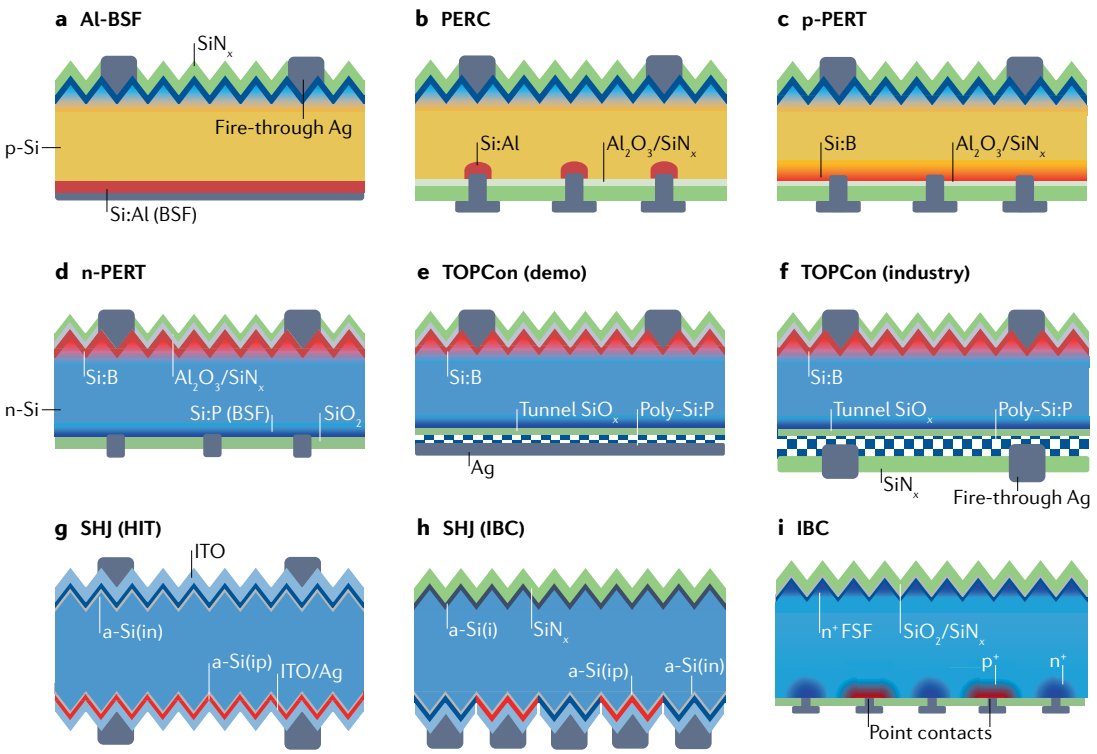


Fig. 3 | **Schematic representation of typical solar cell architectures. a** | A simple cell design based on p-type Si with phosphorus diffusion forming a highly n^+-doped front and full-area Al rear contact forming a highly p^+-doped rear; this type of cell is called Al back-surface field (Al-BSF). **b** | Localized rear contacts in the passivated emitter and rear cell (PERC) architecture. **c**,**d** | Local contacts are also used in passivated emitter and rear totally diffused (PERT) cells, a design that applies to p-type (panel **c**) as well as n-type (panel **d**) wafers. **e**,**f** | n-Type cells with a tunnel oxide passivating contact (TOPCon) design, either with evaporated Ag contact as used in R&D (panel **e**) or with localized fire-through metallization as introduced in industry (panel **f**). **g** | A silicon heterojunction (SHJ) design, also called heterojunction with intrinsic thin layer (HIT), contacted on both sides with intrinsic and doped bilayers (in and ip at front and rear, respectively) and indium tin oxide (ITO). **h** | A rear-contacted SHJ using an interdigitated back contact (IBC). **i** | IBC design with n^+-doped front surface field (FSF) and diffused rear contacts.

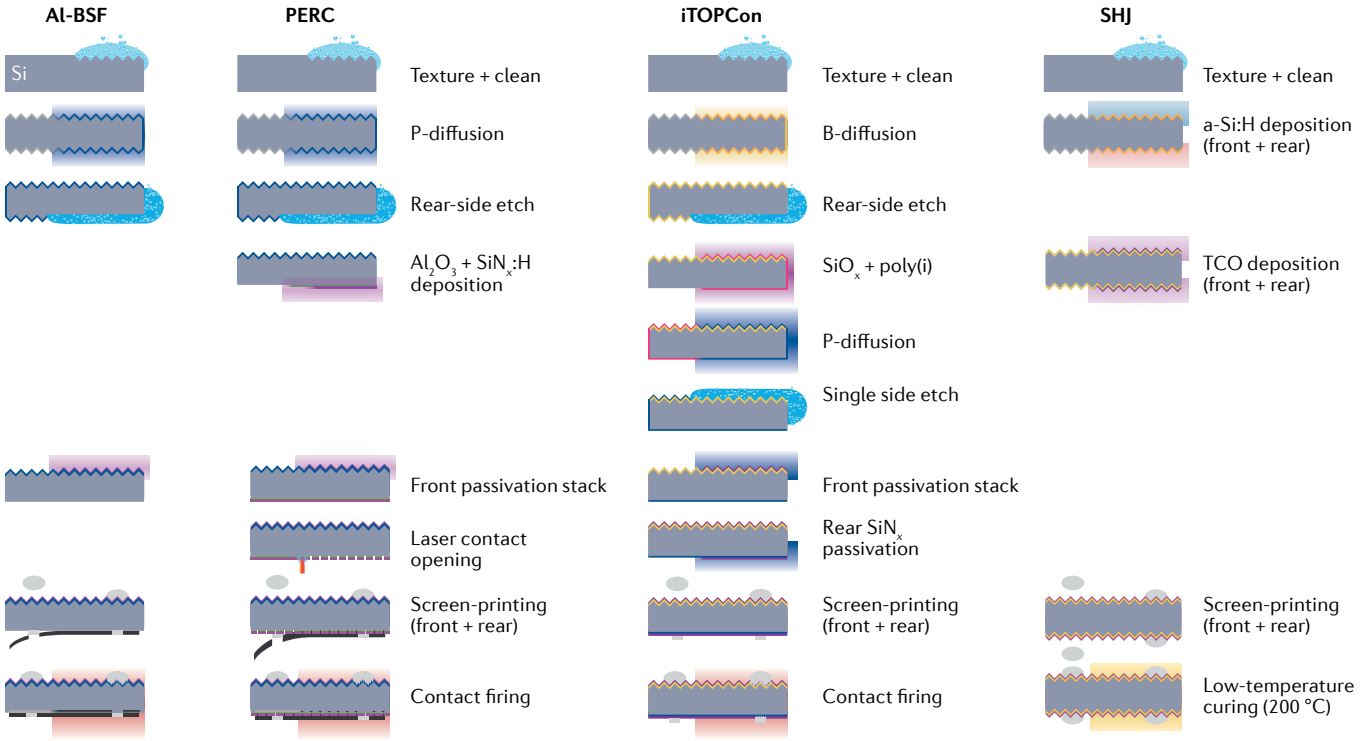


Fig. 4 | **Schematic process flows for the fabrication of solar cells using different architectures.** In most passivated emitter and rear cell (PERC) cells, a 'selective' emitter is created by adding a third step after the phosphorus diffusion, in which the phosphorus glass and crystalline silicon surface are molten by a laser to create a highly doped region in the areas where the metallization fingers are printed later. Note that, despite the simplicity of the silicon heterojunction (SHJ) process flow, production of SHJ cells is currently costlier than that of PERC cells, owing to the use of more expensive equipment, higher material costs and a lower line throughput. BSF, back-surface field; iTOPCon, industrial tunnel oxide passivating contact; TCO, transparent conductive oxide. Adapted with permission from REF.[233], Wiley.

at its surface. The main limitation of Al-BSF solar cells nowadays is, thus, recombination at the full-area rear contact, which limits their efficiency to just above 20%[66].

The PERC architecture (FIG. 3b) lifts this barrier by adding three processing steps (FIG. 4). First, after the emitter diffusion and surface cleaning/back etching, a thin (<2 nm) thermal oxide is grown on both sides of the wafer to improve the surface passivation (not shown on the figure). Second, a thin (<20 nm) Al_2O_3 and a thicker SiN_x:H layer are deposited on the rear of the cell, either by PECVD for both layers or using atomic layer deposition for Al_2O_3 and PECVD for SiN_x:H (REFS[67,68]). Third, the dielectric passivation at the rear is locally opened by laser ablation — recent developments in laser technology helped a lot with the industrialization of this process — before screen-printing of the aluminium paste, either full area or only in finger shapes over the ablated regions for bifacial solar cells. The two main benefits of the PERC design are reduced rear-side recombination, which results in an increased open-circuit voltage, and improved rear reflectivity, which results in an increased short-circuit current (FIG. 5a).

The first efficient cell based on the PERC concept was demonstrated at the University of New South Wales in 1989 (REFS[56,69,70]), using FZ wafers and photolithography-intensive processing. It took over 20 years of collaborations between equipment makers, industry and research institutions to make a cost-effective solar cell from this innovative concept, enabling commercialization of PERC modules in 2010.

As a result of reduced rear recombination, bulk recombination emerged as the main limitation of the PERC cell, triggering interest in high-quality monocrystalline wafers. Unless gallium doping is used, the BO defect is deactivated in an additional step that involves stacking cells onto a carrier that travels through a belt furnace at around 200 °C while maintaining a high forward electrical current through the series-connected cells in the stack. The high temperature and the high carrier concentration injected in the silicon cells increase the diffusivity of hydrogen in silicon. Because the efficiency gain outweighs the cost of the additional processing steps, a fast industrial transition from Al-BSF to PERC took place between 2016 and 2020. At the end of 2020, more than 70% of the cell market was PERC technology and 80% of the wafer market was monocrystalline Cz wafers[10,35], thus, merging the weighted average of FIG. 1c into one single curve towards monocrystalline material. The industrial PERC process enables significantly higher efficiencies, 22–23% on average for monocrystalline Si, with typical record values around 23.5% for a full wafer made on production lines[71–73]. Higher values were reported (for example, 24.0% from LONGi Solar)[74] (FIG. 5b), but without clear indication about the exact contact structure or fabrication environment. Because it contains a local Al-BSF, the industrial 'PERC' cell is,

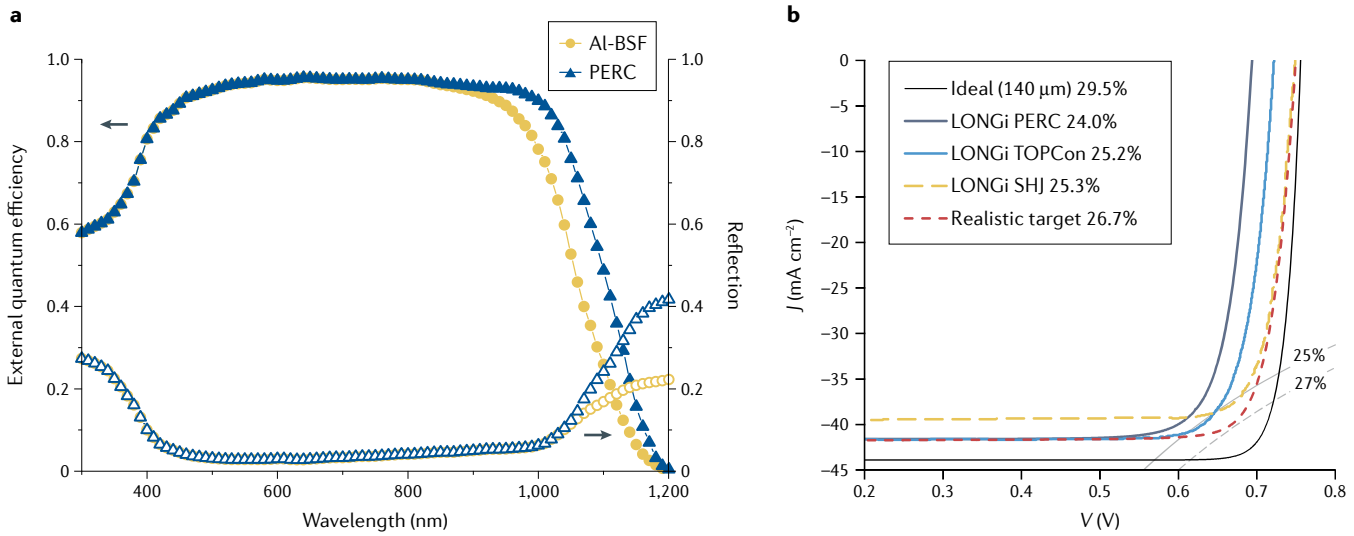


Fig. 5 | **Typical performance characteristics of crystalline silicon solar cells. a** | External quantum efficiency (solid symbols) and reflection (open symbols) for Al-doped back-surface field (Al-BSF, circles) and a passivated emitter and rear contact (PERC, triangles) solar cells. **b** | Current–voltage curves for a PERC cell, a cell with a tunnel oxide passivating contact (TOPCon) and a silicon heterojunction (SHJ) cell compared with the theoretical limit[74,217]. Panel **a** adapted with permission from REF.[234], Wiley.

strictly speaking, a mixture of the PERC and PERL (passivated emitter, rear locally diffused)[75] solar cell concepts. But because this local Al-BSF is alloyed and not diffused, the cell is neither a pure PERC nor a pure PERL cell.

An alternative industrial c-Si cell architecture is the passivated emitter, rear totally diffused technology (PERT)[76] (FIG. 3c,d). This design is particularly interesting for n-type substrates, for which the combined formation of Al-BSF and Al contact is not possible. Instead, it includes both boron diffusion and phosphorus diffusion processes. Owing to their wafer polarity, n-type PERT cells are less prone to boron-related degradation effects and have a higher efficiency potential than p-type PERC cells, owing to a lower sensitivity of the bulk lifetime to some metallic impurities. However, the process complexity is higher and the substrate can be more expensive if a higher initial lifetime is requested.

Shadowing by contacts on the front can be avoided by putting both contact polarities on the rear side of the cell in an interdigitated back contact design[77] (FIG. 3h,i). With this design — and with the use of the passivating contacts described in the next section — the two highest reported designated-area efficiencies are 26.1% for a p-type substrate[78] and 26.7% for an n-type substrate[79]. Back-contacted cells with remarkable total-area efficiencies around 25.0% are successfully commercialized by SunPower Corp. in their high-efficiency modules. Nevertheless, all solar cells with efficiency higher than 25% come at the cost of more complex processing, for example, using photolithography for the definition of the contacts[80]. An important research trend is, therefore, to develop simpler process flows for cell efficiencies above 25%[81–83].

High-temperature passivating contacts

In PERC and PERT solar cells, metal contacts silicon locally on both sides. This leads to significant recombination, limiting the open-circuit voltages. This problem of 'classic metallization' is evident when looking at the highest efficiencies for different cell architectures summarized in TABLE 1. This issue triggered interest in developing passivating contacts, consisting of a layer stack suppressing defects at the silicon surface, yet, ensuring the selective collection of charges towards the metallic electrode. Inspired by the improved properties of Schottky diodes that use a metal–insulator–semiconductor structure rather than a metal–semiconductor one, metal–insulator–semiconductor structures were suggested for solar cells in 1972 (REF.[84]). By 1983, open-circuit voltages as high as 695 mV were demonstrated and, to enhance the compatibility with high-temperature processing, it was proposed to replace the metal by degenerately doped silicon[85]. To improve the efficiency, some research labs still included a slight phosphorus diffusion at the front. In parallel, inspired by research on bipolar transistors with polysilicon emitters, other research teams developed cells using semi-insulating polysilicon[58]. Passivating polysilicon contacts (FIG. 3e,f) became popular after 2010, as they provide surface passivation and tolerate high processing temperatures. They are, thus, compatible with well-established gettering, metallization and hydrogenation processes and, when applied to the full surface, provide good conductivity without crowding the photocurrent into small contact areas[86]. Thus, high-quality monocrystalline wafers and full-area polysilicon contacts form a potentially winning team.

Sandwiched between the wafer and the polysilicon film, a thin layer of silicon oxide has the pivotal role to balance surface passivation and contact conductivity. This oxide layer can be grown chemically[87], a process attractive for industrialization because it can be integrated easily into the wafer-cleaning procedure. The oxide grown this way is generally only 1.0–1.5 nm thick, that is, thin enough for charge carriers to tunnel from the wafer to the polysilicon[88]. Alternatively, thermal

growth of oxides is a standard step in semiconductor processing. The resulting oxides are generally thicker and more stoichiometric, thus, insulating. To establish electrical contact, increasing the thermal budget of subsequent processing steps can be used to open conductive pinholes[89–91]. A layer of highly doped polysilicon can be obtained by low-pressure chemical vapour deposition of an intrinsic layer and subsequent dopant implantation[78] or diffusion[92]. In situ doping is also possible. Alternatively, doped amorphous silicon layers are grown by PECVD[86] or sputtering[93], and subsequently annealed to crystallize them and activate their dopants. Finally, a hydrogenation treatment is commonly applied to passivate defects in the interfacial oxide or at its interface with the silicon wafer.

Different acronyms have been used to name this contact technology. The most commonly adopted one is TOPCon (for tunnel oxide passivating contact)[94], which we use here. Most recent research focuses on n-type polysilicon passivating contacts on the rear side of n-type silicon substrates, using a full-area metallization of evaporated silver. Combined with a boron-diffused junction at the front, the highest reported efficiency for a small-area laboratory cell to date is 25.8% (26% with a rear junction configuration on a p-type wafer)[95]. For upscaling to commercial wafer size, the rear side is generally contacted with an industrial metallization: a layer of SiN_x:H is deposited, followed by screen-printing of a metal grid. In a subsequent firing step, the paste etches through the SiN_x:H to contact the polysilicon film, and hydrogen released from the SiN_x:H passivates interfacial defects. To avoid the metal damaging the oxide layer, the polysilicon thickness has to be over 200 nm (REFS[92,96]). Similar concepts were followed by various industrial

Table 1 | **Highest certified efficiencies of various approaches**

Efficiency (%)	Area (cm^2)	V_{oc} (mV)	j_{sc} ($mA\,cm^{-2}$)	FF (%)	Comment	Refs
Passivating contacts for both polarities in IBCs						
26.7	79.0 (da)	738	42.65	84.9	n-Type, heterojunction IBCs	74,79
26.1	4.0 (da)	726.6	42.62	84.3	p-Type, tunnel oxide IBCs	78
25.0	25.0 (da)	736	41.5	81.9	Tunnel IBC with screen-printing, no lithography	220
25.2	153.5 (ta)	737	41.33	82.7	Exact type of contact not disclosed	221
25.04	243.2 (ta)	715.6	42.27	82.81	n-Type Cz, screen-printed, tunnel oxide electron contact	83
Passivating contacts on both sides						
26.30	274.3	750.2	40.49	86.59	n-Type, a-Si heterojunction, M6 wafer, nine busbars	222
25.1	151 (da)	737.5	40.79	83.5	n-Type, a-Si heterojunction, large area, plated	223
25.26	244.5 (ta)	748.5	39.48	85.46	n-Type, a-Si heterojunction, large area, screen-printed	99
22.6[a]	4.0 (da)	719.6	38.8	80.9	p-Type, tunnel oxide with co-annealed poly contacts, screen-printed	111
Passivating rear contact, 'classic' metal front contact						
26.0	4.0 (da)	732	42.05	82.3	p-Type wafer, n-type TOPCon rear emitter	95
25.8	4.0 (da)	724.1	42.87	83.1	n-Type, front by lithography and plating, n-type TOPCon rear contact	224,225
25.21	243 (ta)	721.6	41.63	83.9	n-Type TOPCon, bifacial, screen-printed	99
Contacted at the front and rear, with 'classic' metal contacts (PERL or PERC design)						
25.0	4.0 (da)	706.0	42.7	82.2	p-Type, metal point contact with local diffusion, original PERL, photolithography, plating	76
24.03	244.6 (ta)	694.0	41.6	83.26	Exact structure not disclosed	226
23.7	261.4 (ta)	692	41.6	82.5	p-Type, full wafer area, screen-printed industrial PERC cell, no selective emitter	227,228
Wafers grown from ingot casting (cast-mono)						
24.4	267.5 (ta)	713.2	41.47	82.5	n-Type, iTOPCon	74
22.8	246.7 (ta)	687.1	40.90	81.2	p-Type, highest monocrystalline cell efficiency in 'mass production', screen-printed	74

After the area, (da) refers to designated area and (ta) to total area[74]. For the different cell designs, see FIG. 3. Note that several higher-voltage devices were reported by multiple companies as 'PERC' structures without clear description. These devices actually include advanced contacting strategies, and they were, thus, disregarded for inclusion in this table as PERC. a-Si, amorphous Si; Cz, Czochralski; FF, fill factor; IBC, interdigitated back contact; iTOPCon, industrial tunnel oxide passivating contact; j_{SC}, short-circuit current density; PERC, passivated emitter and rear cell; PERL, passivated emitter, rear locally diffused; TOPCon, tunnel oxide passivating contact; V_{OC}, open-circuit voltage. [a]Non-certified result.

manufacturers towards a mass production of n-type cells with passivating rear contacts[60,97]. For example, 6" industry cells (FIG. 3f) showed efficiencies of up to 25.25% and an average efficiency of more than 23.5% in production lines, typically resulting in modules with efficiencies of up to 22.5%[83,98–100].

For p-type wafers, the highest reported cell efficiency to date is 26.1%, obtained by combining passivating contacts of both polarities and an interdigitated back contact design[78]. A 26.0% efficiency was reported for a p-type cell contacted on both sides, with a standard (non-passivating) p-type contact at the front and a junction-forming n-type passivating contact at the rear[95]. The formation of p-type contacts is experimentally more challenging than that of n-type contacts, an effect attributed to the higher capture cross section of c-Si–SiO_2 interface states for electrons than holes[101] or to defect creation during the diffusion of boron atoms across the interfacial oxide[102]. The latter can be mitigated by using a boron-free buffer layer on the interfacial oxide[103] or by alloying the boron-doped layer with oxygen, which retards boron diffusion[104]. Alternatively, boron diffusion can be largely reduced by using a low thermal budget to crystallize the silicon layer, as is the case with rapid thermal annealing or co-firing[105].

The design of a high-efficiency solar cell with a TOPCon structure on both sides is still under development. The main difficulty is to combine high transparency, passivation and electrical conductivity on the front side. Current research trends to improve the front TOPCon transparency, besides reducing the thickness of the contact, include localizing the polysilicon only below the metal[106], replacing polysilicon with a more transparent material[107] or alloying polysilicon with oxygen or carbon. Both alloying strategies lead to a trade-off between transparency and conductivity[105,108]. A second difficulty is the application of the TOPCon structure on a textured surface where, once again, p-type contacts are more problematic than n-type contacts[109,110]. The best efficiency reached to date in a device with full-area TOPcon passivating contacts at the front and rear is 22.6%[111].

Low-temperature passivating contacts

An alternative route to form passivating contacts relies on hydrogenated amorphous silicon (a-Si:H). Intrinsic a-Si:H was found to provide a good surface passivation to c-Si as early as 1979 (REF.[112]). The ability to engineer efficient silicon solar cells using a-Si:H layers was demonstrated in the early 1990s[113,114]. Many research laboratories with expertise in thin-film silicon photovoltaics joined the effort in the past 15 years, following the decline of this technology for large-scale energy production. Their success suggests that strong synergies exist between the two fields[57,79,115–118]. A key feature of such silicon heterojunction (SHJ) devices (FIG. 3g,h) is their high V_{oc} (typically 730–750 mV) (TABLE 1). Devices based on heterojunction structures hold the current world record for back-contacted cells at 26.7% efficiency[79] and for large-area wafer screen-printed cells contacted on both sides at 25.3% efficiency[99], with a 2021 record of 26.3% with unspecified metallization (TABLE 1). Several production lines report average efficiency in the range 23.5–24.5% with SHJs.

Among passivation materials, intrinsic a-Si:H has the peculiarities to be a single-phase material with a comparatively narrow bandgap (between 1.6 and 1.9 eV), to contain little to no fixed charge and to provide excellent chemical passivation without any electric field[119]. The narrow bandgap induces small conduction-band and valence-band offsets between the crystalline silicon and a-Si:H. This enables electrons and holes to flow out of the c-Si wafer through relatively thick layers (>10 nm) of a-Si:H without incurring severe resistance. This combination of electrical conductivity and outstanding chemical passivation makes a-Si:H unique and enables its use in passivating contacts.

Similarly to crystalline silicon, a-Si:H can be doped both n-type and p-type using phosphorus and boron. However, doping in a-Si:H is not as efficient as in c-Si, and the electron and hole densities are limited to less than $10^{19}\,cm^{-3}$ in both cases[120]. Because doping inherently creates defects in a-Si:H, doped layers deposited directly onto a c-Si wafer do not provide excellent passivation. Solar cell devices, thus, usually incorporate a thin (<10 nm) layer of intrinsic a-Si:H for surface passivation between the wafer and the doped a-Si:H layers[121–123]. This architecture was initially called heterojunction with intrinsic thin layer (HIT, now a Panasonic trademark)[113] and, nowadays, simply silicon heterojunction. PECVD is the most used deposition method for a-Si:H layers, although hot-wire CVD[124] (and, to a lesser extent, reactively sputtered) a-Si:H films also demonstrated passivation[125,126].

Charge transport in a-Si:H is less efficient than in c-Si, owing to the orders of magnitude lower charge mobilities. As a-Si:H contributes only negligibly to lateral transport of minority carriers towards the front metal grid, an additional transparent conductive oxide layer is typically required. Indium oxide alloyed with tin oxide is mainly used, although other alloying compounds and even indium-free alternatives exist[118,127–131]. Lateral charge transport also occurs in the wafer itself, which relaxes the constraint on the transparent conductive oxide. This is mostly true for electrons owing to the predominant use of n-type wafers, the higher mobility of electrons than holes in Si and the higher contact resistance between the wafer and the electrode for holes, favouring the placement of the electron contact on the illuminated side of the device[132]. Approaches that do not include a transparent conductive oxide, although technically possible[133,134], are not yet used, because direct metallization of a-Si:H films is delicate. Arguably, together with the wider bandgap, the low mobility of a-Si:H contributes to enabling very thin layers to efficiently 'screen' the influence of the electrode to ensure passivation and carrier selectivity[135], leading to highly efficient solar cells with a-Si:H stacks of about 10 nm on each side.

Optically, the small bandgap of a-Si:H induces parasitic light absorption when using a-Si:H as a window contact. Whereas all light absorbed in the doped layer is lost for photocurrent, part of the light absorbed in the intrinsic layer can contribute to the photocurrent[136]. The search for alternative contact layers providing

improved transport and transparency is currently very active. Nanocrystalline silicon (showing a better transparency and doping efficiency than a-Si:H) and thin-film silicon alloys are natural directions for improvements[137–142]. Promising alternative materials include transition-metal oxides, but this research remains academic so far, with an uncertain path for industrialization[143–149]. At this time, only MoO_x exhibits similar efficiencies as p-doped a-Si:H for the hole-selective contact and TiO_x for the electron-selective contact[148,150,151]. In the latter case, a full-area aluminium layer acting as metal electrode contributes to the electron selectivity of the contact stack. The mandatory use of such metal electrodes in the case of electron contacts using non-silicon-based materials precludes their use on the light-incoming side of solar cells. Although an efficiency up to 23.1% has been demonstrated using a localized silicon-free electron contact[152], most of the highly efficient devices using metal oxides as passivating contacts still include an intrinsic a-Si:H passivation layer. This layer is, so far, required to reach excellent open-circuit voltages (typically >700 mV) with low-temperature approaches. Efficiencies above 21% (two-side contacted) and 22% (all-rear contacted) were demonstrated in 'dopant-free' architectures (not using doped silicon to form the contact)[153,154]. Parasitic light absorption in a-Si:H is totally eliminated in interdigitated back contact devices, for which even light absorbed in a front intrinsic a-Si:H layer contributes to photocurrent[116,153,155]. This structure has enabled the highest efficiency silicon solar cells since 2015 (REFS[116,156]). Process complexity precludes industrialization, but significant simplifications of the manufacturing process were demonstrated[81,82].

In all approaches involving a-Si:H, the post-a-Si:H processing steps must be kept below 200–250 °C: hydrogen effusion at temperatures above 200 °C leads to a performance drop (mostly through loss of passivation). This effect can be mitigated[157,158] and even reversed up to temperatures as high as 400 °C (REF.[159]), but above 450 °C, the passivation ability of a-Si:H is irremediably lost. Consequently, silver screen-printing pastes cannot be fired at high temperatures like in standard cell processing, instead requiring the use of low-curing-temperature pastes. This fundamental difference distinguishes SHJ contacts (also called low-temperature passivating contacts) from TOPCon contacts. Despite remarkable progress, the low-temperature silver pastes are still a factor two to three more resistive than high-temperature ones, resulting in a higher consumption of silver than for PERC cells with an equivalent metallization pattern[160,161]. However, multi-busbar or proprietary approaches such as SmartWire enable a reduction of the silver cost[82]. The limitation to low processing temperatures also prevents wafer bulk improvement by high-temperature impurity gettering (except as an extra step before a-Si deposition[162]). Low processing temperatures, however, enable the use of thinner wafers compared with standard PERC technology, down to below 100 µm (REFS[57,163,164]). Originally, only n-type wafers with long carrier lifetime were considered for SHJ technology, but similar efficiencies have since been demonstrated for high-quality p-type and n-type wafers[115,165,166].

Minimizing cell-to-modules losses

Moving from individual wafers to full modules, there is a systematic difference between the module power and the sum of the power of individual cells. The ratio of these powers is called the cell-to-module (CTM) power ratio, and is usually around 95–97%. Similarly, the module efficiency is lower than the average cell efficiency, leading to a CTM efficiency ratio of typically 85–90%. The evolution over the past 20 years in wafer size, shape and interconnection is illustrated in FIG. 6. After decades of fairly standardized wafer and module sizes, 2019 saw a paradigm shift, with the emergence of larger wafers and more aggressive assembly techniques. This change in industry targets aimed at increasing the CTM efficiency ratio, as high module efficiency translates to savings on module costs and installation costs per W. Assuming a configuration with five busbars (FIG. 6b, 2017 design), monocrystalline 156 × 156-mm² PERC cells with 22.44% efficiency would typically lead to a 60-cell module[10] sized 1.7 m² with 19.5% efficiency (FIG. 6a, top). Using the same cell efficiency but applying a module design illustrative of the trends of 2021 (210 × 210-mm² cells cut in three and reassembled with an improved interconnection scheme in a larger module of 2.4 m²) (FIG. 6b, 2021 design) can lead to state-of-the-art PERC modules with an efficiency of 21% (FIG. 6a, bottom), an increase of the CTM efficiency ratio from 87% to 93%.

Considering the importance of module design changes for increasing the efficiency, we describe here the origin of module losses and the mitigation pathways to reduce them. The factors contributing to module losses are broken into three broad categories: geometric, optic and electric factors (FIG. 6a), and their contributions are obtained using the software SmartCalc.CTM.

The main CTM loss is geometric and originates from the non-unity coverage of cells in the module (the coverage is only ~90% of the total area for typical modules). This loss accounts for more than 1.5% of the absolute efficiency difference, but it is not accounted for when calculating power CTM loss, explaining its higher value. Optical losses are due to the reflection of light at the air–glass interface, to the differences in reflection between a cell in air and a cell embedded in the encapsulation, to absorption losses in the encapsulation and to extra shadowing from interconnection ribbons or wires. Optical gains also occur, because part of the light reflected from the fingers, interconnection ribbons and backsheet in the space between cells can be internally reflected at the glass–air interface, giving it another chance to be absorbed in the cells[167]. Finally, electrical losses come from the cells' electrical interconnection.

Improvements in the stringing of cells (series interconnection of multiple cells) enabled the move from typically two or three 1.5-mm-wide busbars in 2012 to five or six 0.9-mm-wide busbars in 2014. Most recent high-efficiency modules incorporate 9 to 12 busbars or even up to 18 to 21 wires[168]. Although this increase usually does not change the CTM ratio, it shortens the finger length, which decreases series resistance at the cell level and enables the use of thinner fingers (resulting in lower silver paste consumption and lower shadowing), improving the cell and, thus, module, cost and performance[169,170].

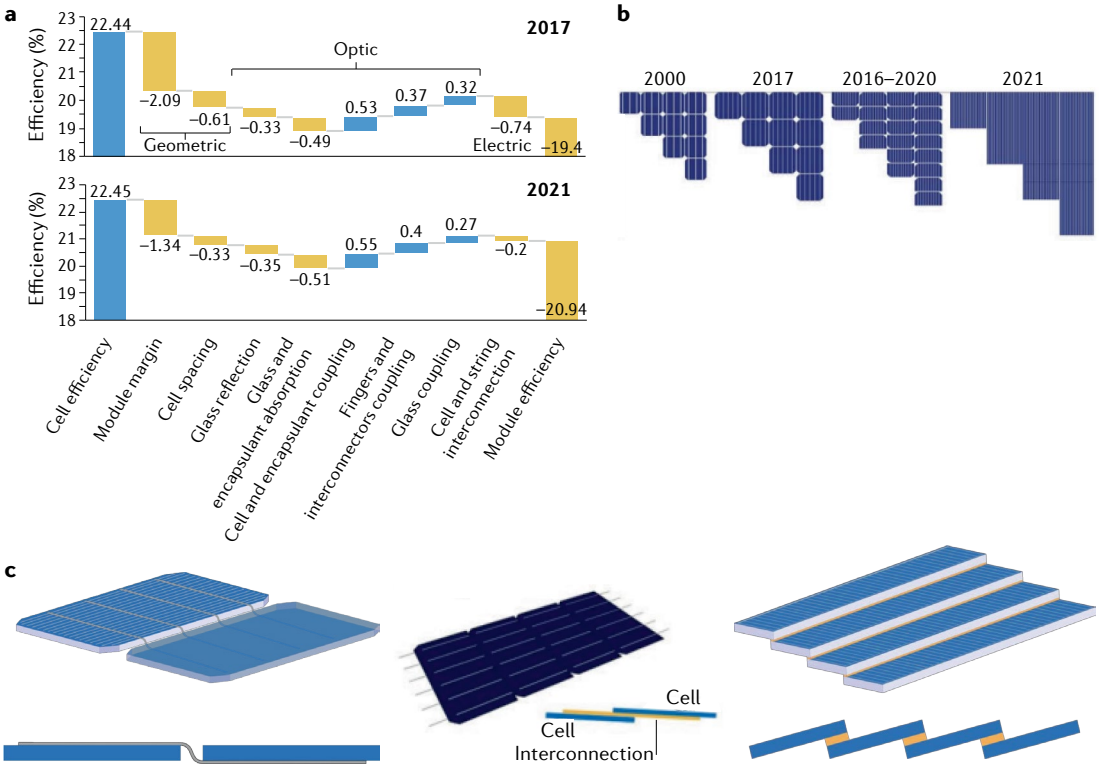


Fig. 6 | **From cells to modules. a** | Typical cell-to-module loss analysis performed with the modelling package SmartCalc.CTM for a 2017 premium module scheme of 1.7 m^2 consisting of 60 156-mm pseudo-square wafers connected with five busbars (top), as in panel **c**, left, and for a 2021 module of 2.4 m^2 consisting of 150 third-cut 210-mm full-square wafers connected with nine busbars (bottom) with tiling of the cells, as in panel **c**, middle. The main improvements lay in the area coverage (first two elements) and in the interconnection (last element). **b** | Evolution of standard module design from the years 2000 to 2021. The first sketch represents 125-mm quasi-square wafers using three busbars and standard interconnection (panel **c**, left). The second sketch shows 156-mm quasi-square wafers with five busbars, which was standard in 2017, corresponding to the first cell-to-module analysis shown in panel **a**. The third sketch shows 156.75-mm half-cut quasi-square wafers with nine busbars, which is illustrative of the 2016–2020 evolution. The last sketch represents one of many of 2021's options with 210-mm third-cut full-square wafers using tiling ribbon interconnections (panel **c**, middle). Quasi-square wafers prevent material waste when cutting a square from a cylindrical ingot: 150-mm-diameter ingots were typically used for 125-mm-wide wafers, moving to 200-mm and 210-mm diameters for wafers 156 mm and 156.75 mm wide, respectively. The latter size enables wafers with a lower fraction of lost area in the missing corners, but a larger share of the ingot discarded. **c** | Sketches of the interconnection for the two modules compared in panel **a**, using standard interconnections (left) and a tiling ribbon design (middle), and of the interconnection for shingled modules (right). Panel **c** (right and left) adapted with permission from REF.[235], Fraunhofer ISE http://www.metallizationworkshop.info/fileadmin/layout/images/Konstanz-2017/MWS2017/VIII_4_Klasen.pdf. Panel **c** (middle) adapted with permission from REF.[236], LONGi.

Increasing the wafer size is attractive because it improves the productivity of cell and module lines and reduces the loss due to cell spacing in the module. However, larger wafers produce more current, which increases the electrical losses for a given interconnection. Cutting the cells in half reduces the interconnection losses by a factor of four[171,172]. Assembling a PV module with series and parallel interconnections from half-cut cells also makes the module more tolerant to partial shading and improves its reliability against hotspots[173]. Most of the PV industry has, thus, switched to larger size (with typically 166-mm, 182-mm or 210-mm lateral wafer sizes) and half-cell modules in 2020. The cell cutting process is critical and must be tailored to minimize edge defects and maintain high performance, especially for high-efficiency devices based on materials with long carrier lifetimes and, thus, diffusion lengths. The significant series-resistance reduction at the module level can outbalance a moderate loss in cell efficiency upon cutting[174]. This effect is particularly marked in standard test conditions corresponding to full-sun illumination (thus, for the rated module power), but is more questionable for lower illumination conditions, under which the decrease of series resistance has less impact. Thus, the gain in performance is obvious for sunny locations, but smaller for temperate climates.

Innovative designs aiming at suppressing the gap between cells to improve module efficiencies are explored by many companies[175]. In the shingle design, the wafer is cut into multiple slabs along the edge of the busbars. Slabs are then assembled similarly to shingles on a roof, with each busbar hidden under the adjacent cell and the electrical contact formed by conductive adhesive (FIG. 6c, right). Challenges include reliability

and yield, owing to the overlap of the cells[176–179], and silver paste consumption, owing to the long fingers. An innovative tiling ribbon solution, potentially alleviating these limitations, was recently proposed by several companies. It uses half or third wafers interconnected with multi-busbars that are flattened at the point of overlap[175], thereby, creating a negative gap between consecutive cells (FIG. 6c, middle).

Noticeably, most commercial modules incorporate an anti-reflection coating on the glass, typically consisting of a porous glass layer with a low refractive index. This layer reduces the weighted solar reflection at the air–glass interface from 4% to about 1.3–2% for normal incidence, and greater benefits are obtained at oblique incidence angles[180,181].

Inside the laminate, the light reflected by the interconnecting ribbons can be largely recovered if the surface of the ribbons is grooved and, thus, reflects light at an oblique angle, enabling total internal reflection at the glass–air interface and absorption in the cell. The rounded shape of wire interconnects — which are becoming standard — partly enables this effect.

Combining several approaches, optical gains can compensate optical and electrical losses, leading to CTM power ratios over 100%[174,182]. Nevertheless, the CTM efficiency ratio always remains below 100%, mainly owing to the fact that the module area is larger than the total cell area. Overall, cost remains the main driver for large-scale production and decides on the implementation of many advanced strategies that are already technologically demonstrated.

Continuous industry improvements

Average module efficiency is increasing by about 0.3–0.4% absolute per year and this trend is accelerating with the transition to mono c-Si and novel module design[10] (FIG. 1c). Efficiency increases will continue in the coming decade, at the end of which the maximum practical efficiency for single-junction silicon modules (23–24% for mainstream and possibly 25% for high-end modules) should be reached through the sets of improvements we described (better material, improved passivation, better contacting pastes, modified/improved cell structures including passivating contacts, modified module assembly).

In parallel, reliability continues to be of paramount importance, as reducing the expected annual degradation rate lowers the calculated levelized cost of electricity. Based on past experience and accelerated testing, many manufacturers offer warranties of 25 years or even 30 years on the product performance, usually within a linear (relative) degradation of typically 0.5–0.7% per year. Besides the aforementioned degradation of the bulk silicon material, c-Si modules are subject to various degradation modes. The potential difference between the (grounded) outside of the module and the wafers in high-voltage strings can lead to potential-induced degradation[183–185]; UV light induces yellowing of the polymers; thermal and mechanical stress can crack cells and interconnections; corrosion can degrade contacts; encapsulants can delaminate; and so on[186]. These effects can be minimized by either cell-level modification (for example, using denser Si-rich silicon nitride layers to prevent potential-induced degradation) or module-level modifications, such as using encapsulating polymers and backsheets that are more resistive and more stable to UV light. Some technology-specific degradation mechanisms also exist. For example, a few studies have reported a slightly higher degradation rate for SHJ modules fabricated in the early 2000s than for modules made with standard multi-crystalline BSF cells from the same period[187–190]. It can be expected that new technologies showing higher performance are more prone to degradation, thus, requiring dedicated strategies for high reliability that were not necessary (thus, not introduced) 5–10 years ago[191–193]. The maturation of such strategies will likely be hastened by the large-scale industrial adoption of passivating contact technologies, enabling these modules to reach similar — or even improved — reliability compared with today's standard.

The International Electrotechnical Commission (IEC) testing standards, such as IEC 61215, define standard procedures to detect design and manufacturing flaws in PV modules. However, they are not designed to guarantee a 25-year or 30-year lifetime of the module in every climate, as they do not reproduce accurately the reality in the field. Harder testing sequences, with longer cycles and stricter criteria (such as UV, heat and current flow) are frequently used in the industry to give manufacturers better insurance that their warranty is valid, especially when changing materials or suppliers to achieve better efficiency or lower cost. Reliability testing must always remain a major concern when establishing large solar parks with investments of several hundreds of millions of dollars, and the science of the reliability of PV modules is continuously developed to improve the predictability of failures[187,194]. On a positive note, several evaluations of systems that are more than 20 years old show that most modules still perform well past their expiration date[194]. However, these old-technology modules were produced with very different materials and designs from today's standards, precluding a complete extrapolation of these results.

One such increasingly popular design is bifacial modules. Such modules can provide more annual energy per rated W than monofacial ones by enabling light absorption from both sides. Bifacial modules are gaining a larger market share despite slightly higher manufacturing costs[195–197]. This bifacial gain, which is also valid for tracking systems, depends on the performance under back-side illumination. The bifaciality factor, the ratio of rear-illuminated efficiency to front-illuminated efficiency, ranges from 70–75% for p-type PERC to 96% for n-type SHJ cells, and the additional energy yield, typically around 5–15%, depends on the design and arrangement of the module arrays, on the location and on the ground albedo.

In 2020, large solar power plants (>10 MW) can be installed for around US$0.5 W^{-1} in several countries, and solar electricity costs through power purchase agreements are reported below US$0.02 kWh^{-1} for large solar farms located in sunny countries and US$0.047 kWh^{-1} in Germany[198–200]. Anticipating further module cost reductions (−30% relative), module efficiency increases

(+20% relative) and improvements in solar park mounting and configuration (bifacial modules, higher voltage, improved energy yield), a further 30% solar electricity cost reduction is expected within the next decade, leading power purchase agreements to routinely reach US$0.013–0.03 kWh^{-1} in most areas in the world. This estimate is based on a reduction of module and inverter costs of 30% and a reduction of area-related costs by 30% (10% linked to the learning curve and 20% to efficiency increases and an energy yield increase by 9% attributed to bifaciality and improved temperature coefficient).

To meet the objective of the 2015 Paris Agreement and keep the average temperature increase of the Earth below 2 °C, the global emissions of greenhouse gases must be brought down to zero by mid-century. Photovoltaics can play a central role in the transformation of the energy economy. Depending on the scenario, powering the world with sustainable electricity would typically require over 40–70 TW of global installed PV capacity[1,201,202], which means reaching an annual production volume of 1.5–3 TW per year within the next decade, and then keeping a stabilized production of several TW per year until 2050 (REF.[203]). Reaching an annual production target of 2 TW by 2030 would require a 30% annual volume growth from 2020 levels (estimated at 140 GW). Such 30% annual growth was noteworthily achieved — on average — during the past decade (13 GW in 2011 to 140 GW in 2020). In a less optimistic scenario, an annual growth of 16% would bring the annual production rate to 600 GW per year by 2030, but would require to increase the production of PV modules to a much higher level than in the previous scenario to meet the objectives by 2050; this scenario bears the risk of an overshoot in production capacity after 2050 (REF.[203]).

In all growth scenarios, most of the observed historical trends are expected to continue. For mainstream modules, price pressure will force all stakeholders in the supply chain to reduce their cost, inciting them to minimize the consumption of energy and material, notably by using thinner wafers, less silver, possibly substituted with copper, and less packaging material, while improving module efficiency. Even with conservative estimates for the annual growth in production (16%) and for the price learning curve (18%), a further cost reduction of 30–40% can be expected by 2030 (BOX 1). We can expect that the impressive reduction of investment costs (capital expenditure, CAPEX) along the full chain (FIG. 1b) will continue. Noticeably, the CAPEX for a 10-GW (of annual production) PERC solar cell fabrication (from wafer to cells) decreased, in the past 6 years, from around US$1.2–1.5 billion to US$280 million if sourced in China[201,204,205]. At this level, depreciated over 6 years, the impact of CAPEX for a cell line accounts for as little as US$0.005 W^{-1}. Since higher-efficiency products (interdigitated back contact or SHJ cells) require, so far, higher CAPEX investments, PV companies targeting fast volume growth have favoured PERC cells in the past few years.

Alternative technologies to silicon

With close to 95% of market share in 2020, a well-established supply chain and a standardized design, silicon dominates the PV industry. Although other PV technologies have potential advantages (such as reduced material usage for thin films), taking up large market shares is challenging for them because they have to demonstrate better price and/or efficiency than silicon, with at least the same reliability. The thin-film technologies based on copper indium gallium selenide or CdTe have already demonstrated module efficiencies above 19%[10]. Based on the demonstrated cell efficiencies, a similar performance could be expected for perovskites, and a better one in tandem configuration. Other mature technologies, such as thin-film silicon, have been discarded owing to fundamental efficiency limitations (below 15%), and alternative technologies such as polymer or dye-sensitized solar cells do not yet have the efficiency level to enter the mainstream market. CdTe PV modules could, so far, keep up with the drastic price reduction in silicon PV modules. However, the availability of tellurium will most likely become a limitation for multi-TW annual volumes[206]. The best single-junction solar cell efficiency for unconcentrated light is currently obtained with thin GaAs devices with a record value of 29.1%. Estimated production costs are, however, more than 100 times higher than for a traditional silicon PV module, forcing the recent stop of the only pilot module manufacturing line[207]. Any new single-junction technology trying to enter the market within the next 5–10 years will be restricted to niche markets (high power density, lightweight, building cladding, automotive). Yet, for c-Si mass production, a solar cell efficiency of 26% is considered by many as a practical limit. An open question is, thus, what could come next in terms of efficiency.

Today, the only proven concept to further increase efficiency is the combination of solar cells in a multi-junction configuration. Using silicon as a bottom cell, 4-terminal tandem devices have shown up to 32.8% efficiency (GaAs on Si) and 4-terminal triple-junction devices reached 35.9% efficiency (GaIn/GaAs on Si)[208]. Monolithic wafer-bonded triple junctions reached 33.3% efficiency[209], whereas direct epitaxy of III–V on silicon led, so far, to efficiencies over 25%[210,211]. Yet, the high cost of growing high-quality III–V thin films will (at best) restrict such devices to niche markets for several years[208].

Currently, the most promising route for high-efficiency and low-cost photovoltaics is the monolithic integration of a perovskite top cell on a silicon bottom cell. In 2018, the first tandem devices with efficiency over 25% were reported[212–215]. A couple of devices surpass 29% efficiency[216,217] and the best certified 4-cm^2 device surpasses 26%[218], all of them using a SHJ bottom cell. The module-level efficiency potential for such devices is over 30%, and even higher with triple-junction configurations, which allows for higher module cost when considering the full PV system[219]. A swift industry adoption could happen through an upgrade of existing Si module production lines with the tools needed for a perovskite top cell, similar to the extraordinarily fast evolution from Al-BSF to PERC cell production. The major challenge will be the demonstration of reliable products, as perovskite devices are particularly sensitive to intrinsic and extrinsic degradation mechanisms, including by contact with air moisture, by exposure to

UV light and high temperature or by electrical biasing. Eventually, the combination of high-bandgap and low-bandgap thin-film solar cells (such as perovskite/perovskite) could combine high efficiency and low cost, spelling the death of crystalline silicon PV technology. Nevertheless, beyond competition, synergetic progress of all PV technologies is welcome to meet the objective of 100% renewable energy by 2050.

Conclusions

Silicon photovoltaics has moved at an impressively fast pace to reduce cost, with steady efficiency gains at the cell and module level for commercial products. Many advanced R&D efforts are still ongoing to further improve silicon material and decrease its cost, as well as to improve cell manufacturing, through sharpening current industry-standard processes or developing low-cost approaches and hardware for the realization of next-generation products incorporating passivating contacts. Combined with the improvements in module technology (larger area, half-cells, tiling ribbons, shingled cells, multi-wires, back-contacted approaches), this will ensure a further reduction of the efficiency gap between today's record laboratory c-Si solar cells and mainstream modules.

With crystalline silicon occupying a large part of the market and continuously improving, it will be challenging for other technologies to gain or maintain a large market share. Except for niche applications (which still constitute a lot of opportunities), the status of crystalline silicon shows that a solar technology needs to go over 22% module efficiency at a cost below US$0.2 W^{-1} within the next 5 years to be competitive on the mass market. Higher-efficiency approaches, which command a price premium because of area-related system costs, could be obtained by combining silicon with higher-bandgap top cells, with perovskite being the main candidate for absorber.

Silicon PV devices can be made, even at the TW scale, without any rare or scarce materials, and substitution materials can be used for critical elements (for example, silver has been replaced with copper and indium with zinc and/or tin in SHJ cells). At the unbeatable electricity price level discussed here, there is room for managing solar electricity (long-distance transport, demand-side management, electrochemical storage) and for its transformation into heat, cold or chemicals, such as through power-to-gas processes (H_2, NH_3 and so on), in an economically sustainable way. Hence, there is no technological limitation to provide the amount of electricity and energy the world needs to make the necessary transition to renewable energy, and political will and economic levers are currently the main roadblocks. The silicon PV industry has gone, in the past three decades, from a curiosity in the energy sector to being "the new king of electricity", as stated by the International Energy Agency. Photovoltaics will play a central role in decarbonizing the global energy economy and mitigating climate change, and silicon technology will remain a key player for the next several decades.

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